What is claimed is:

1. A method for fabricating a capacitor formed on a substrate wherein said capacitor is utilized in a semiconductor device, said method comprising the steps of:

designating a salicide gate for use with said semiconductor device;

configuring a self-aligned contact for use with said semiconductor device; and

combining said salicide gate and a self-aligned contact in a memory cell area of said semiconductor device to thereby permit the efficient shrinkage of memory cell size without an additional mask or weakening of associated circuit performance.

2. The method of claim 1 further comprising the steps of:

patterning a poly gate on said substrate with a hard mask; and

performing a cell implant thereof.

3. The method of claim 2 further comprising the step of:

depositing TEOS, SiN, BPTEOS on said substrate; and

performing an IPO-1 planarization upon a layer formed on said substrate.

4. The method of claim 3 further comprising the step of:

performing an anisotropic etch back thereof to stop on said poly gate utilizing high selectivity between said poly gate and said anisotropic etch back, wherein said anisotropic etch back comprises anisotropic etch back based on a combination of oxide and SiN.

5. The method of claim 4 further comprising the steps of:

defining a logic poly gate;

performing an LDD implant upon said substrate; and

forming a spacer deposition layer upon said substrate.

6. The method of claim 5 further comprising the steps of:

performing a spacer TEOS dry etch followed by a stop at SiN;

utilizing an additional photo mask to open an associated DRAM array; and

utilizing a wet dip upon said substrate and said layers thereof to remove a spacer TEOS.

7. The method of claim 6 further comprising the steps of:

performing a spacer SiN dry etch upon said substrate and said layers thereof followed by a stop on a TEOS; and

utilizing a wet dip upon said substrate and said layers thereof to remove said spacer TEOS.

8. The method of claim 7 further comprising the step of:

defining an RPO upon said substrate; and

forming a Co-salicide upon said substrate for use with said semiconductor device.

9. The method of claim 8 further comprising the step of:

utilizing said capacitor formed between a metal-one layer and a metal-two layer upon said substrate in said semiconductor device, wherein said capacitor comprises an MIM capacitor.

10. The method of claim 1 wherein said semiconductor device comprises a DRAM-based semiconductor device.

11. The method of claim 2 wherein said poly gate comprises a DRAM poly gate.

12. The method of claim 2 wherein said cell implant comprises a cell LDD implant.

13. The method of claim 1 wherein said capacitor comprises an MIM capacitor.

14. A method for fabricating a MIM capacitor upon a substrate, wherein said MIM capacitor is utilized in a DRAM-based semiconductor device thereof, said method comprising the steps of:

patterning a DRAM poly gate upon said substrate with a hard mask;

performing a cell LDD implant upon said substrate;

depositing TEOS, SiN, and BPTEOS layers upon said substrate;

forming a IPO-1 planarization layer upon said substrate;

performing an anisotropic etch back upon said substrate and layers thereof to stop on said poly gate utilizing high selectivity between said poly gate and said anisotropic etch back, wherein said anisotropic etch back comprises anisotropic etch back based on a combination of oxide and SiN;

defining a logic poly gate upon said substrate and layers thereof;

performing an LDD implant upon said substrate and layers thereof;

performing a spacer deposition upon said substrate and layers thereof;

performing a spacer TEOS dry etch followed by a stop at SiN upon said substrate and layers thereof;

utilizing an additional photo mask to open an associated DRAM array;

utilizing a wet dip upon said substrate and layers thereof to remove a spacer TEOS;

performing a spacer SiN dry etch upon said substrate and layers thereof followed by a stop on a TEOS;

utilizing a wet dip upon said substrate and layers thereof to remove said spacer TEOS.

defining an RPO upon said substrate and layers thereof; and

forming a Co-salicide upon said substrate and layers thereof for use with said semiconductor device.

utilizing said capacitor between a metal-one layer and a metal-two layer upon said substrate and layers thereof, wherein said capacitor comprises an MIM capacitor.

15. A system for fabricating a capacitor formed on a substrate wherein said capacitor is utilized in a semiconductor device, said system comprising:

a salicide gate designated for use with said semiconductor device, wherein said salicide gate is formed upon said substrate and layers thereof;

a self-aligned contact configured for use with said semiconductor device, wherein said self-aligned contact is formed upon said substrate and layers thereof; and

said salicide gate and said self-aligned contact combined in a memory cell area of said semiconductor device upon said substrate and layers thereof to thereby permit the efficient shrinkage of memory cell size without an additional mask or weakening of associated circuit performance.

16. The system of claim 15 further comprising:

a poly gate patterned with a hard mask upon said substrate and layers thereof; and

a cell implant upon said substrate and layers thereof.

17. The system of claim 16 further comprising:

depositions of TEOS, SiN, BPTEOS formed upon said substrate and layers thereof; and

an IPO-1 planarized layer thereof.

18. The system of claim 17 further comprising:

an anisotropic etch back that stops on said poly gate, wherein said anisotropic etch back is performed utilizing high selectivity between said poly gate and said anisotropic etch back, such that said anisotropic etch back comprises anisotropic etch back based on a combination of oxide and SiN.

19. The system of claim 18 further comprising:

a logic poly gate defined upon said substrate and layers thereof;

an LDD implant; and

a spacer deposition layer formed upon said substrate and layers thereof.

20. The system of claim 19 further comprising:

a spacer TEOS dry etch followed by a stop at SiN upon said substrate and layers thereof;

a photo mask which may be utilized to open an associated DRAM array; and

a wet dip upon said substrate and layers thereof, wherein said wet dip removes said spacer TEOS.

21. The system of claim 20 further comprising:

a spacer SiN dry etch performed upon said substrate and layers thereof followed by a stop on a TEOS; and

a wet dip which removes said spacer TEOS performed upon said substrate and layers thereof.

22. The system of claim 21 further comprising:

an RPO defined upon said substrate and layers thereof; and

a least one Co-salicide formed upon said substrate and layers thereof for use with said semiconductor device.

23. The system of claim 22 further comprising:

said capacitor formed between a metal-one layer and a metal-two layer in said semiconductor device upon said substrate and layers thereof, wherein said capacitor comprises an MIM capacitor.

24. The system of claim 15 wherein said semiconductor device comprises a DRAM-based semiconductor device.

25. The system of claim 16 wherein said poly gate comprises a DRAM poly gate.

26. The system of claim 16 wherein said cell implant comprises a cell LDD implant.

27. The system of claim 15 wherein said capacitor comprises an MIM capacitor.

28. A system for fabricating a MIM capacitor utilized in a DRAM-based semiconductor device, said system comprising:

a DRAM poly gate patterned with a hard mask upon said substrate and layers thereof;

a cell LDD implant;

TEOS, SiN, and BPTEOS deposition layers formed upon said substrate and layers thereof;

an IPO-1 planarized layer formed upon said substrate and layers thereof;

an anisotropic etch back formed upon said substrate and layers thereof which stops on said poly gate, wherein said anisotropic etch back is performed utilizing high selectivity between said poly gate and said anisotropic etch back, such that said anisotropic etch back comprises an anisotropic etch back based on a combination of oxide and SiN;

a logic poly gate defined upon said substrate and layers thereof;

an LDD implant;

a spacer deposition layer formed upon said substrate and layers thereof;

a spacer TEOS dry etch followed by a stop at SiN upon said substrate and layers thereof;

a photo mask which opens an associated DRAM array;

a wet dip upon said substrate and layers thereof which removes a spacer TEOS;

a spacer SiN dry etch performed upon said substrate and layers thereof followed by a stop on a TEOS;

a wet dip performed upon said substrate and layers thereof, wherein said wet dip removes said spacer TEOS.

an RPO defined upon said substrate and layers thereof;

a Co-salicide formed for use with said semiconductor device upon said substrate and layers thereof.

said capacitor formed between a metal-one layer and a metal-two layer upon said substrate and layers thereof, wherein said capacitor comprises an MIM capacitor.